DS 11: Symposium: New Materials for Nanoelectronics

Time: Tuesday 9:30–13:15 Location: H32

Invited Talk DS 11.1 Tue 9:30 H32

Strained silicon for advanced nanotechnology — •Michael Goryll[1], Dan Buca[1], Qing-Tai Zhao[1], Bernd Holländer[1], Siegfried Mantl[1], Roger Loo[2], Duy Nguyen[2], and Manfred Reiche[3] — [1]Institut für Bio- und Nanosysteme (IBN1) und cni, Forschungszentrum Jülich, D-52425 Jülich, Germany — [2]IMEC, Kapeldreef 75, B-3001 Leuven, Belgium — [3]MPI für Mikrostrukturphysik, Weinberg 2, D-06120 Halle, Germany

Introducing strain into silicon layers has shown carrier mobility increase in CMOS devices. Two prevailing approaches, the global strain and the local strain platform, will be presented. While in case of local strain, small-area selective epitaxial SiGe growth is employed, global strain presents more challenges regarding layer deposition. We will discuss our approach towards global strain based on thin pseudomorphic SiGe layers, that are being strain relaxed using He^+ ion implantation and thermal annealing. The morphology and crystallinity of the layers was investigated using optical microscopy, atomic force microscopy and transmission electron microscopy. Characterization methods employed to determine the residual strain in the silicon layers comprise angular ion beam scanning and Raman spectroscopy. Strained silicon on insulator (sSOI) layers were produced by layer transfer to an insulating substrate. This process includes wafer bonding as well as splitting performed by H_2^+ ion implantation and annealing. Electrical measurements on n-channel MOSFETs fabricated on this sSOI material will be presented that exhibit the expected electron mobility enhancement.

Invited Talk DS 11.2 Tue 10:00 H32

Integration of functional epitaxial oxides into silicon: From high-K application to nanostructures — •H. Jörg Osten — Institut für Materialien und Bauelemente der Elektronik, Leibniz Universität Hannover, Appelstr. 11A, 30167 Hannover

There are several attempts to increase the material variety that is compatible with Si technologies. The ability to integrate crystalline dielectric barrier layers into silicon structures can open the way for a variety of novel applications ranging from high-K replacements in future MOS devices to oxide/silicon/oxide heterostructures for nanoelectronic application in future quantum-effect devices. First, we will demonstrate and discuss the epitaxial growth of oxides on different oriented Si substrates based on surface and interface considerations. Here, we will present results for crystalline lanthanide oxides on silicon in the cubic bixbyite structure grown by solid state MBE.

Experimental results for Gd_2O_3-based MOS capacitors show that these layers are excellent candidates for application as very thin high-K materials replacing SiO_2 in future MOS devices. In addition, we will present a new approach for nanostructure formation which is based on solid-phase epitaxy of the Si quantum-well combined with simultaneous vapor-phase epitaxy of the insulator on top of the quantum-well. Ultra-thin single-crystalline Si buried in a single-crystalline insulator matrix with sharp interfaces was obtained by this approach on Si(111). Finally, the incorporation of crystalline Si islands into single-crystalline oxide layers will be demonstrated.

Invited Talk DS 11.3 Tue 10:30 H32

Rare Earth based amorphous ternary oxide layers as alternative gate dielectrics — •Jürgen Schubert[1], Tassilo Heeg[1], Martin Roeckerath[1], Joao Marcelo Jordao Lopes[1], Uffe Littmark[1], Chao Zhao[2], Matty Caymax[2], Valerie Avanasiev[3], Lisa Edge[4], Yunfa Jia[4], Wei Tian[4], and Darrell Schlom[4] — [1]IBN 1-IT and CNI, Forschungszentrum Jülich GmbH, 52425 Jülich — [2]IMEC, Kapeldreef 75, B-3001 Leuven, Belgium — [3]Department of Physics, University of Leuven, Celestijnenlaan 200D, B-3001 Leuven, Belgium — [4]Penn State University, 16802 University Park, Pennsylvania, USA

Rare Earth based oxide thin films are promising candidate materials to replace SiO_2 as a gate dielectric in MOSFETs of the next generation. So far most attention attracted HfO_2 and Hf-containing silicates but they have severe drawbacks such as too low recrystallization temperature ($T_{cr} = 600°C$). Calculations on the thermal stability of ternary oxides in direct contact with silicon were resulted in a number of more appropriate oxides [1]. E.g. $GdScO_3$ single crystals showed excellent properties which could be reproduced for amorphous films. Permittivity of 22, a bandgap of 5.6 eV, band offsets larger than 2 eV and a good thermal stability ($T_{cr} > 900°C$) could be verified. Furthermore those oxides are not hygroscopic in contrast to most of the binary systems. Another promising system is $LaLuO_3$ which shows k-values of 32 combined with a high thermal stability ($T_{cr} > 900°C$). Most recent results will be presented and discussed. [1] D.G. Schlom and J. Haeni, MRS Bulletin V. 27, No. 3 (2002)

Invited Talk DS 11.4 Tue 11:00 H32

Advanced SOI CMOS transistors for high performance microprocessors — •Manfred Horstmann — AMD Saxony LLC & Co. KG, Wilschdorfer Landstrasse 101, 01109 Dresden, Germany

An overview of state of the art advanced Silicon on Insulator CMOS transistors used for high performance microprocessors will be given. For advanced SOI transistors stress engineering has become a standard feature since the 90 nm technology node due to gate oxide scaling limitations [1]. Especially techniques to induce local strain like compressive and tensile stressed over-layer films, embedded-SiGe, and stress memorization are keys to maintain transistor performance. With optimization, the different stressors are highly compatible and additive to each other, improving PMOS and NMOS saturation drive current by ca. 50 % and 30 %, respectively. This results in 40 % higher product speed. In addition to reduce the lateral and vertical device dimensions advanced Laser or Flash) annealing has been applied [2]. These anneal processes yield an improved dopant activation for active and gate regions resulting in lower source-drain resistance and gate depletion without any additional diffusion. These techniques have been applied and optimized for 90 nm and 65 nm volume manufacturing and are scaleable to 45 nm design rules. Technology options for future transistors like Strained Silicon directly bonded on SOI, fully depleted SOI, High K or FinFETs will be discussed.

[1] M. Horstmann, et al., IEDM 2005, p. 243 [2] Th.Feudel et al., RTP Conference, Kyoto, 2006

DS 11.5 Tue 11:30 H32

Herstellung und Charakterisierung von MOSFETs mit Gadoliniumscandat als alternatives Gatedielektrikum — •Martin Roeckerath, Joachim Knoch, Joao Marcelo Jordao Lopes, Tassilo Heeg, Jürgen Schubert und Siegfried Mantl — Institut für Bio- und Nanosysteme (IBN 1 - IT) und CNI, Forschungszentrum Jülich, D-52425 Jülich, Germany

Seltene-Erd-Scandate sind durch ihre herausragenden morphologischen und elektrischen Eigenschaften eine vielversprechende Materialklasse für die Verwendung als High-k-Dielektrikum in zukünftigen CMOS Anwendungen. Speziell $GdScO_3$ weist eine hohe thermische Stabilität sowie eine DK von ca. 23 auf. In dieser Arbeit wurde dieses Material nun in Feldeffekt-Transistoren (MOSFETs) als alternatives Gateoxid integriert. Besonderer Schwerpunkt der Untersuchung lag auf dem Einfluss der High-k-Silizium-Grenzfläche auf die elektrischen Eigenschaften der Bauelemente. Das Oxid wurde mittels Elektronenstrahlverdampfen von stöchiometrischem Quellenmaterial im Hochvakuum hergestellt. Um die Grenzfläche zu variieren wurde das $GdScO_3$ sowohl auf chemischem Oxid als auch auf wasserstoffterminierter Si(100)-Oberfläche abgeschieden und einige Proben außerdem nachträglich in Sauerstoff getempert. Die elektrische Charakterisierung der Bauelemente zeigt einen deutlichen Einfluss sowohl des Temperns als auch der Vorbehandlung auf deren Ströme sowohl im Aus- als auch im Anzustand. Außerdem kann eine Schwellspannungsverschiebung beobachtet werden. In diesem Beitrag wird auch der Einfluss der Grenzflächeneigenschaften auf die Ladungsträgerbeweglichkeit diskutiert.

Invited Talk DS 11.6 Tue 11:45 H32

Graphene: A new Electronic Material — •Max Christian Lemme[1], Tim Echtermeyer[1], Matthias Baus[2], and Heinrich Kurz[1,2] — [1]Advanced Microelectronic Center Aachen (AMICA), AMO GmbH, Otto-Blumenthal-Str. 25, 52074 Aachen, Germany — [2]Institut für Halbleitertechnik, RWTH-Aachen, Sommerfeldstr. 24, 52074 Aachen, Germany

Carbon based electronics offer one of the most promising options to enhance silicon CMOS technology in the future. Great attention has been paid to carbon nanotubes (CNTs) because of their intriguing electronic properties. Their application in electronics, however, will depend strongly on the availability of self organizing processes. Graphene

films, monolayers of carbon, have only recently been identified as a new contender for carbon electronics. Graphene's planar form predestinates it as a booster for silicon technology. In this talk, field effect devices (FEDs) manufactured from few- and monolayer graphene are presented. Except for graphene deposition, only conventional top-down CMOS-compatible processes have been used. Raman spectroscopy is presented as the method of choice for distinguishing few- from monolayer graphene. Electron and hole mobilities in graphene pseudo-MOS structures are compared to those obtained from double-gated Graphene-FEDs. Even when covered by silicon oxide, the values exceed the universal mobility of silicon and silicon-on-insulator MOSFETs.

Invited Talk DS 11.7 Tue 12:15 H32

Electronic Transport in Carbon Nanotube FETs — •Joachim Knoch — IBM Research GmbH, Zurich Research Laboratory, Säumerstrasse 4, 8803 Rüschlikon, Switzerland

Carbon nanotubes have recently attracted a great deal of interest due to their unique structural and electronic properties. In particular, carbon nanotube field-effect transistors have been widely investigated as an alternative for future nanoelectronics applications. In the present talk we will discuss the electronic transport properties of CNFETs.

Usually, contacts are formed by depositing metals on top of the nanotube. One focus of the talk will be the investigation of the role of these source/drain contacts on the device behavior. As it turns out, CNFETs behave similarly to ultrathin-body Schottky barrier MOSFETs. Although the ultrathin diameter (body) allows for an excellent carrier injection through the Schottky-barrier, its presence prohibits the observability of multi-mode transport in such CNFETs. Details regarding multi-mode transport and the role of scattering for the visibility of multi-mode transport will be discussed. Furthermore, we will present CNFETs with 'doped' source/drain contacts and study the relevant phenomena occuring in such conventional-type devices. A charge pile-up in case of short channel devices deteriorates the device performance and leads to large off-state leakage currents. Finally, a new device architecture based on band-to-band tunneling is introduced which allows to combine an excellent on-state performance with a switching ability superior to any conventional FET. It will be shown that one-dimensional objects are ideally suited for the realization of such tunneling FETs.

DS 11.8 Tue 12:45 H32

Strukturierte Schichtsysteme für horizontal gerichtetes Wachstum von Kohlenstoff-Nanoröhren — •Matthias Büenfeld[1], Bernd Schröter[1], Frank Schmidl[1], Matthias Grube[1], René Geithner[2], Thomas Pertsch[1], Detlef Schelle[2], Wolfgang Richter[1], Andreas Tünnermann[2] und Paul Seidel[1] — [1]Institut für Festkörperphysik, Friedrich-Schiller-Universität, Jena, Germany — [2]Institut für Angewandte Physik, Friedrich-Schiller-Universität, Jena, Germany

Kohlenstoff-Nanoröhren ermöglichen durch ihre Form und Größe sehr interessante Anwendungen. Das gerichtete Wachstum ist für solche Anwendungen ein grundlegender Aspekt. Ziel ist es, die Nanoröhren gezielt horizontal auf Oberflächen wachsen zu lassen. Dabei bieten sich unterschiedliche Einflussmöglichkeiten. Für das Wachstum der Nanoröhren sind Katalysatorpartikel im nm-Bereich (im wesentlichen Eisen, Nickel oder Kobalt) notwendig. Vorstrukturierung dieser Materialien und die Größe dieser Partikel haben wesentlichen Einfluss auf den Durchmesser und das Wachstum der Nanoröhren. Durch Kombination unterschiedlicher, strukturierter Oxidschichten sind weitere Auswahlkriterien für Wachstumsort und Wachstumsrichtung gegeben.

DS 11.9 Tue 13:00 H32

Determination of the coefficient of thermal expansion (CTE) of porous dielectric films using x-ray reflectometry — •Sebastian Taube, Holm Geisler, Ulrich Mayer, Inka Zienert, Michael Hecker, and Ehrenfried Zschech — AMD Saxony LLC & Co. KG, Wilschdorfer Landstr. 101, D-01109 Dresden, Germany

In advanced integrated circuits thin interlayer dielectric (ILD) films with reduced relative permittivity (k) will be used for reducing crosstalk and interconnect signal delay. It is the final goal to achieve as small as possible k-values which are close to the physical limitation ($k_{vacuum} = 1$). For reaching lowest possible k values, new materials or nano porous layers are potential candidates. However, these layers have many different properties in comparison with the traditionally used silica glass, e.g., considerably reduced mechanical stiffness. The CTE value is one important property of such an ILD layer. The advanced integrated circuits undergo during the fabrication and later in the practice permanent changing temperature cycles. Thin film stacks with relatively large differences in the CTE of the individual thin films are a reliability concern for microelectronic products. The thickness of a thin film as well as the variation of the thickness due to increased temperature can be measured very precisely with XRR. It will be shown here that the CTE of (ultra) low-k layers can be determined for relevant process and application temperatures with the XRR method. The measured CTE values are typically higher than for metals, e.g., copper.