HL 49 Devices

Time: Thursday 15:15–16:30 Room: BEY 154

HL 49.1 Thu 15:15 BEY 154

80 GHz Passive Mode Locking of InGaAs Quantum Dot Lasers Emitting at 1.3 μm — •Gerrit Fiol[1], M. Kuntz[1], F. Hopfer[1], M. Lämmlin[1], C. Szewc[1], D. Bimberg[1], A.R. Kovsh[2], and N.N. Ledentsov[1,2] — [1]Technische Universität Berlin, Institut für Festkörperphysik, PN 5-2, Hardenbergstrasse 36, 10623 Berlin, Germany — [2]NL Nanosemiconductor GmbH, Konrad-Adenauer-Allee 11, 44263 Dortmund, Germany

The sample structure incorporating a 15-fold stack of InGaAs QDs emitting at 1.3 μm was grown by MBE. The wafers were processed into two-sectional ridge waveguide structures with a 20 μm gap between the sections to ensure good electrical insulation. All samples were mounted p-side up and were electrically contacted with a two-channel probe head. The section lengths of the devices were 1800/200 μm for the 20 GHz device, 900/100 μm for the 40 GHz device and 450/50 μm for the 80 GHz device. An autocorrelator was used to measure the pulse width. The 20 GHz device was passively mode-locked. The shortest deconvoluted pulse width best fitted by a sech2 shaped pulse was 900 fs, which is the shortest pulse width for all devices we investigated. The 40 GHz device was hybridly and passively mode-locked. The deconvoluted pulse width ranged from 1.8 to 6 ps with a time-bandwidth-product of $\Delta\tau\Delta\nu$=0.72 for the shortest pulse width. The locking range for hybrid mode locking was 7 MHz at a RF power of 7dBm. The minimum pulse width we achieved at 80 GHz was 1.5 ps. The corresponding spectrum yields a time-bandwidth product of 1.7, which is well above the Fourier transform limit of 0.32.

HL 49.2 Thu 15:30 BEY 154

Comparison of carbon nanotube field-effect-transistor architectures: Schottky-barrier, conventional and tunneling CNFETs — •Joachim Knoch[1], Joerg Appenzeller[2], Yu-Ming Lin[2], Zhihong Chen[2], and Phaedon Avouris[2] — [1]Institute of Thin Films and Interfaces, ISG1-IT, Forschungszentrum Juelich, D-52425 Juelich — [2]IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, USA

Carbon nanotube field-effect-transistors (CNFETs) have recently attracted an increasing attention as building blocks of a future nanoelectronics and tremendous progress towards a real application has been made. Here, we present experimental as well as simulation results on three different CNFET device designs: the Schottky-barrier CNFET (SB-CNFET) with metallic source/drain contacts, the conventional CNFET (c-CNFET) with doped source/drain electrodes and the tunneling CNFET (t-CNFET) based on band-to-band tunneling. While a c-CNFET, in principle, exhibits a superior on- and off-state performance if compared to SB-CNFET it is shown that ultimately scaled c-CNFETs suffer from a charge pile-up that strongly deteriorates the device's off-state. In contrast, the t-CNFET allows for an excellent off-state. Due to the smallness of nanotubes (both, in terms of geometry as well as the one-dimensionality of electronic transport properties) the t-CNFET design makes possible field-effect transistor devices with an inverse subthreshold slope significantly smaller than 60mV/dec while at the same time, an excellent on-state is achievable.

HL 49.3 Thu 15:45 BEY 154

Hydrogenated Microcrystalline Silicon Thin Film Transistors — •Kah-Yoong Chan[1,2], Eerke Bunte [1], Helmut Stiebig[1], and Dietmar Knipp [2] — [1]Research Center Jülich, Institute of Photovoltaic, 52425 Jülich, Germany — [2]International University Bremen, School of Engineering and Science, 28759 Bremen, Germany

Hydrogenated microcrystalline silicon (μc-Si:H) has recently been proven to be a promising material for thin film transistors TFTs. Electron carrier mobility of >100cm2/Vs, deconvoluted from μc-Si:H TFT characteristics has been demonstrated [1]. The high carrier mobility and good stability of the transistors is caused by the presence of crystalline silicon domains with a typical crystal diameter of 5-20nm. In our study, we developed top-gate staggered μc-Si:H TFTs on glass substrate using plasma enhanced chemical vapor deposition (PECVD). Device structures were fabricated by photolithography ranging from 10μm to 100μm channel length and 100μm to 1000μm channel width. The electrons were injected in the channel via 30nm thick n-type μc-Si:H layer. The thin n-type film prepared at ˜280°C exhibits room temperature dark conductivity of ˜10S/cm and an activation energy of ˜17meV. The channel of the transistor was formed by intrinsic μc-Si:H prepared at ˜200°C in the regime near the transition to the amorphous growth (crystalline volume fraction > 50%). The dielectric was realized by PECVD deposited SiO2 film at ˜150°C. The fabrication process together with first experimental results from the electrical characterizations of the μc-Si:H TFTs will be presented. 1. C-H. Lee, A. Sazonov, A. Nathan, Mater. Res. Soc. Symp. Proc. Vol. 862 (2005) A17.5.1-6.

HL 49.4 Thu 16:00 BEY 154

Impact of the body thickness on the performance of silicon-on-insulator Schottky-barrier metal-oxide-semiconductor field-effect-transistors — •Joachim Knoch[1], Min Zhang[1], Siegfried Mantl[1], and Joerg Appenzeller[2] — [1]Institute of Thin Films and Interfaces, ISG1-IT, Forschungszentrum Juelich, D-52425 Juelich — [2]IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, USA

Schottky-barrier MOSFETs are an attractive alternative to conventional MOSFETs. Due to metallic electrodes in direct contact with the channel they offer low extrinsic parasitic resistances, excellent scalability down to smallest dimensions and easy processing. However, because of the Schottky barriers, SB-MOSFETs show an inferior intrinsic performance in terms of Ion/Ioff if compared to conventional devices: A high SB not only deteriorates the transistor's on-state but also causes a poor subthreshold behavior. Here we present experimental and simulation results on ultrathin body (UTB) SOI SB-MOSFETs and show that the use of UTB SOI strongly improves the devices on- as well as off-state. An analytical approximation for the off-state is given that shows that the inverse subthreshold slope scales as the square-root of the SOI thickness. In addition, threshold voltage variations that appear in UTB SOI SB-MOSFETs will be discussed. Two different mechanisms are responsible for this, namely the above mentioned strong dependence of the device performance on the SOI thickness and vertical quantization due to the confinement of carriers between the gate and the buried oxide. Design rules are given of how to avoid too large threshold voltage variations and at the same time achieve a good device performance.

HL 49.5 Thu 16:15 BEY 154

Dynamic and static properties of quantum-dot based semiconductor optical amplifiers at 1.3 μm — •Matthias Lämmlin[1], G. Fiol[1], M. Kuntz[1], F. Hopfer[1], N.N. Ledentsov[1,2], A.R. Kovsh[2], A. Jacob[3], A. Umbach[3], and D. Bimberg[1] — [1]Institut fuer Festkoerperphysik, Technische Universitaet Berlin, PN5-2, Hardenbergstr. 36, 10623 Berlin, Germany — [2]NL Nanosemiconductor GmbH, Konrad-Adenauer-Allee 11, 44263 Dortmund, Germany — [3]u2t Photonics AG, Reuchlinstrasse 10/11, 10553 Berlin, Germany

Quantum dot (QD) based semiconductor optical amplifiers (SOAs) operating at 1.3 μm grown by molecular beam epitaxy containing InGaAs/GaAs QDs are presented. Static gain properties of SOAs based on 10 stacks of QDs are evaluated with respect to input power, wavelength and injection current. Measurements show a chip gain up to 24 dB with a signal-to-ASE ratio of 30 dB. The polarization dependence of these devices shows a TE/TM ratio of 8 dB. Gain measurements of SOAs (15 stacks of QDs, 4 mm long) are compared with a rate equation model. A chip gain of 26 dB is realized here. The modeling of the gain characteristics of these SOAs is matched to the performance of alike lasers and predicts a 40 dB amplification under ideal biasing and input power conditions. Using a hybrid mode-locked QD laser at 20 GHz with 710 fs pulse widths as input signal ultrafast amplification with no observable degradation of the amplified ultrashort pulse train is demonstrated. This work is funded by the SANDiE Network of Excellence of the European Commission, contract number NMP4-CT-2004-500101, and the State of Berlin in the framework of the Zukunftsfond Berlin (TOB).